NEW PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

TACHIBANA, et al. Atty. Dck. No.: 100353-00185

Serial No.: Unknown Examiner: Unknown

Filed: March 25, 2004 Art Unit: Unknown

For: SEMICONDUCTOR INTEGRATED CIRCUIT

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450 Date: March 25, 2004

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the information items listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each item is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the items be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date, OR (b) before the mailing date of a first Office Action on the merits in the present application, OR (c) accompanies a Request for Continued Examination.. No certification or fee is required.

☐ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

☐ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☐ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

☐ c. A check in the amount of $180.00 in payment of the fee under 37 CFR §1.17(p). Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300 as needed to ensure consideration of the disclosed information.

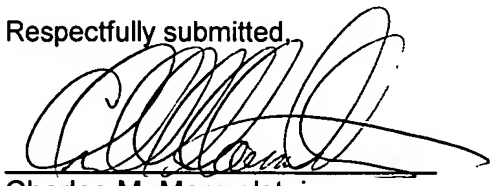
☐ 3. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Applicant(s) hereby petition(s) that the Information Disclosure Statement be considered. Attached is our check in the amount of $180.00 in payment of the petition fee under 37 CFR §1.17(i)(1). Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300 as needed to ensure consideration of the disclosed information.

☐ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☐ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

☒ 4. English-language Abstracts of the non-English language references are attached hereto.

Respectfully submitted,



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LIST OF REFERENCES CITED BY APPLICANT		APPLICANT TACHIBANA, et al.	
(Use several sheets if necessary)		FILING DATE March 25, 2004	GROUP Unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	NO	PART.
	AF	05-204479	August 13, 1993	Japan					X
	AG	06-309052	November 4, 1994	Japan					X
	AH	08-186484	July 16, 1996	Japan					X
	AI	10-198447	July 31, 1998	Japan					X
	AJ	2001-147725	May 29, 2001	Japan					X
	AK	2002-99336	April 5, 2002	Japan					X
	AL	2003-78366	March 14, 2003	Japan					X

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AM	G. Tzanateas, C.A.T. Salama, and Y.P. Tsividis, "A CMOS Bandgap Voltage Reference," IEEE Journal of Solid-State Circuits, Vol. SC-14, No. 3, pp. 655-657, June 1979
	AN	K.N. Leung, and P. K. T. Mok, "A Sub-1-V 15-ppm/°C CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Devices," IEEE Journal of Solid-State Circuits, Vol. 37, No. 4, pp. 526-530, April 2002
	AO	A. Boni, "Op-Amps and Startup Circuits for CMOS Bandgap References With Near 1-V Supply," IEEE Journal of Solid-State Circuits, Vol. 37, No. 10, pp. 1339-1343, October 2002
	AP	H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, pp. 670-674, May 1999

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.